

22. The unpredictable microprocessor or microcomputer according to claim 20, further including means (R1, R2, R3) for de-correlating the running of the programs from an isochronous clock.

23. The microprocessor or microcomputer according to claim 20, characterized in that the main program can enable or inhibit the switching mechanism or mechanisms by loading the switching circuit (53) for switching and enabling the working memories (51, 52) and blocks of storage registers (54, 55) associated with each respective working memory (51, 52), and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program.

24. The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the second working memory (52) and its access registers (A3, D3) are substituted for the working memory (51) and its access registers (A2, D2) in utilization by a main program.

25. The unpredictable microprocessor or microcomputer according to claim 22, characterized in that the de-correlating means comprise a random number generator (2) for triggering, via an interrupt circuit (4), a random interrupt for desynchronizing the running of the programs in the processor, by randomly jumping to the secondary program (P2).

26. The microprocessor or microcomputer according to claim 23, characterized in that the de-correlating means comprise a time counting system (R3) independent from the processor (1) for, after the time count, triggering an interrupt for returning from the secondary program to the main program.

27. The unpredictable microprocessor or microcomputer according to claim 23, characterized in that the means (53, 54, 55, A2, A3, D2, D3) for switching working memories is controlled by the processor and its program, by the random interrupt system (2, 4), by a timer (R3), or by any combination of at least two of the three named elements.

28. The unpredictable microprocessor or microcomputer according to claim 20, characterized in that the means (53, 54, 55, A2, A3, D2, D3) for switching working memories is enabled

4 by being loaded by the processor (1) running a main program
5 sequence.

1 29. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that the secondary
3 program (P2) uses a working space identical to that of the main
4 program (P1) in the main memory (6).

1 30. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that the secondary
3 program (P2) uses a working space smaller than that of the main
4 program.

1 31. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that the switching
3 means carry out the substitution of the memories (51, 52, 53,
4 54, 55, A2, A3, D2, D3) and the associated contexts within the
5 execution cycle of an instruction from the microprocessor.

1 32. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that the secondary
3 program (P2) does not modify the general operating context of
4 the main program (P1) in order to allow the main program to
5 return without having to reestablish said context.

1 33. The unpredictable microprocessor or microcomputer
2 according to claim 32, characterized in that the context of the
3 main program (P1) is reestablished either automatically by the
4 secondary program (P2) or automatically by the switching means
5 (53) before returning control to the main program (P1).

1 34. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that it further
3 comprises means for substituting the memory of the secondary
4 program (P2) for the memory of the main program (P1).

1 35. The unpredictable microprocessor or microcomputer
2 according to claim 20, characterized in that the main program
3 (P1) can use the first working memory (51) and/or the second
4 working memory (52) alternately or simultaneously.

1 36. The unpredictable microprocessor or microcomputer
2 according to claim 23, characterized in that loading of the
3 switching circuit (53) makes it possible to mask or unmask de-
4 correlating interrupts.

1 37. The unpredictable microprocessor or microcomputer,
2 according to claim 25, characterized in that an interrupt

3 triggered by the secondary program (P2) effects return to the
4 main program (P1) after the switching register (53) has been
5 properly loaded, by executing an instruction of the main
6 program (P1) or the secondary program (2), in order to unmask
7 the interrupts.

1 38. The unpredictable microprocessor or microcomputer,
2 according to claim 20, characterized in that the microprocessor
3 or microcomputer is embodied in a monolithic integrated
4 circuit.

1 39. Unpredictable microprocessor or microcomputer
2 according to claim 21, further including means (R1,R2,R3) of
3 de-correlating the run-through of the programs with respect to
4 an isochronal clock.

1 40. Microprocessor or microcomputer according to claim 21
2 characterized in that the main program is adapted to enable or
3 inhibit the switching mechanism or mechanisms by loading the
4 switching circuit (53) of working memories (51, 52) and of the
5 memorization register blocks (54,55) associated with each
6 respective working memory (51, 52)

1 41. Unpredictable microprocessor or microcomputer
2 according to claim 21 characterized in that the second working
3 memory (52) and the associated access registers (A3,D3) of the
4 second working memory are adapted to be replaced in the use
5 thereof by a main program, with said first memory (51) and the
6 associated access registers (A2,D2) of the first memory.

1 42. Unpredictable microprocessor or microcomputer
2 according to claim 22 characterized in that the
3 de-correlating means comprise a random generator.

1 43. Microprocessor or microcomputer according to claim 25
2 characterized in that the means of de-correlation include a
3 time counting system (R3) independent of the processor (1) for
4 enabling, at the end of a time count, the triggering of an
5 interruption to return from the secondary program (P2) to the
6 main program (P1).

1 44. Unpredictable microprocessor or microcomputer
2 according to claim 25 characterized in that the means of
3 switching (53, 54, 55, A2, A3, D2, D3) the working memories is
4 controlled, either by one of the microprocessors and the
5 program thereof, the random interruption system (2,4), a time

6 counter (R3), or a combination of at least two out of the three
7 named elements.

1 45. Microprocessor or microcomputer according to claim 22
2 characterized in that the main program is adapted to enable or
3 inhibit the switching mechanism or mechanisms by loading the
4 switching circuit (53) of working memories (51,52) and of the
5 memorization register blocks (54,55) associated with each
6 respective working memory (51,52).

1 46. Unpredictable microprocessor or microcomputer
2 according to claim 22 characterized in that the second working
3 memory (52) and the associated access registers (A3,D3) of the
4 second working memory are adapted to be replaced in the use
5 thereof by a main program, with said first memory (51) and the
6 associated access registers (A2,D2) of the first memory.

1 47. Unpredictable microprocessor or microcomputer
2 according to claim 26 characterized in that the means of
3 switching (53, 54, 55, A2, A3, D2, D3) the working memories is
4 controlled, either by one of the microprocessors and the
5 program thereof, the random interruption system (2,4), a time

6 counter (R3, or by a combination of at least two out of the
7 three named elements.

1 48. Unpredictable microprocessor or microcomputer
2 according to claim 25 characterized in that the interruption
3 circuit (9) triggers the random generator to thereby trigger
4 the random interrupt to desynchronize execution of the programs
5 in the processor, by random connection to the secondary program
6 (P2).

1 49. Unpredictable microprocessor or microcomputer
2 according to claim 26 characterized in that the de-correlation
3 includes a time counting system (R3) independent of the
4 processor (1) for enabling, at the end of a time count, the
5 triggering of an interruption to return from the secondary
6 program (P2) to the main program (P1), and the means of
7 switching (53, 54, 55, A2, A3, D2, D3) the working memories is
8 controlled by one of the microprocessors and the program
9 thereof, the random interruption system (2,4), a time counter
10 (R3) or by a combination of at least two of the three named
11 elements.

1 50. Unpredictable microprocessor or microcomputer
2 according to claim 21 characterized in that the means of

